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10/032,058	12/31/2001	Katsuyuki Yonezawa	SON-2307	5643

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EXAMINER
ENGLUND, TERRY LEE

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,058	YONEZAWA, KATSUYUKI	
	Examiner	Art Unit	
	Terry L Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2002 and 02 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5 and 7-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 7-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *02 December 2002* is: a)☒ approved b)☐ disapproved by the Examiner

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment/Drawings

The amendment and drawings submitted on Dec 2, 2002 were reviewed and considered with the following results:

Amended Figs. 6, and 13-15 overcame their respective objection described in the previous Office Action. Also, the amended paragraphs on pages 16-18 overcame the objection to Figs. 3 and 4. Therefore, all of the drawing objections have now been withdrawn.

The amended changes to the disclosure overcame its objections that were described in the previous Office Action. Those objections have also been withdrawn.

The cancellation of claims 4 and 6 rendered their respective objections and rejections moot.

Amended claims 1, 5, and 7 overcame their respective objections, which have been withdrawn.

The rejection of claim 2 under 35 U.S.C. 112, first paragraph has been withdrawn. After reconsidering the amended claim, the comments, and the applicant's figures, claim 2 is now considered misleading. Since the applicant's comments did not sufficiently clarify what type of series connection is actually meant with respect to the circuits' connections between the first and second power supplies, a rejection of claim 2 is described below under 35 U.S.C. 112, second paragraph. Related comments are described under the Response to Arguments section.

The rejections of claims 3, 8, and 9 under 3 5 U. S. C. 112, second paragraph, as described in the previous Office Action, have been withdrawn. However, the amended claims,

especially the addition of a plurality of first and second differential circuits to independent claim 1, created numerous new rejections. These are described later under the appropriate section.

Although section "3." of the amendment's page 10 cites "Claims 6, 8, and 9 are canceled", the amendment clearly shows claims 8 and 9 have been amended. Therefore, they are still considered active within the present application.

The prior art rejections of claims 1-3, 5, and 7-9 under 35 U.S.C. 103(a), with respect to Mihailovits et al., have been withdrawn. However, new rejections are described later, under the appropriate section, to account for the amended claim language, and to include a reference to help support the examiner's contention that parallel connected transistors (or diode-connected transistors) can be used in place of a single transistor (or diode-connected transistor) with an emitter area of n.

Claim Rejections under 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 1-3, 5, and 7-9 are rejected under 35 U. S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The series connections within claims 1-3 are confusing. For example, it is not clear how the first/second series connection circuits of claim 1 relate to the current through the capacitor, their connection between the input/output terminals, and/or their connection between the first/second power supplies. Is the capacitor's current only related to just one each of the first/second currents within the plurality of first/second differential circuits and the current source's current, or is the capacitor's current related to all the currents with respect to

the plurality of differential circuits within the first/second series connection circuits? As presently understood, it is not clear how a plurality of first (and second) differential circuits are connected in series between first and second power supplies as recited within claim 2 if each differential circuit retains its own connection of one electrode to a first electrode as lines 2-11 of claim 1 recite. For example, is the plurality of first differential circuits actually connected in series between the power supplies, or is the claim misleading, wherein the first differential circuits are connected between the power supplies, but the first differential circuits are actually connected in series with respect to the filter circuit's input/output terminals (e.g. see 15A2-1, 15A2-n, 11, 18, 13, and 14 of the applicant's own Fig. 7)? It is not clear how "a plurality of said first differential circuits", "a circuit input terminal'", and "a circuit output terminal" within claim 3 (lines 2-4) relate to "a plurality of said first differential circuits", "a circuit input terminal", and "a circuit output terminal" as now recited within claim 1 (lines 19-26). For example, is the plurality of first differential circuits cited within claim 3 referring to a smaller plurality of circuits within claim 1's first series connection circuit, and are the input/output terminals of the circuit related to the terminals of the filter circuit, either one of the series connection circuits, or perhaps to specific differential circuits? It is not understood in claim 3 how the singular "said second differential circuit" relates to the "number of said second differential circuits", and the "second series connection circuit" now recited within claim 1. For example, lines 19-22 of claim 1 already indicate the second differential circuits are connected in parallel with the first differential circuits. Therefore, they are known to be parallel to at least their respective first differential circuit. It is not clear in claim 5 how the one and four transistors, the four and one diodes, the first circuit input terminal, and the first circuit output terminal relate to the plurality

of transistors and diodes, and the circuit input/output terminals recited within claim 1. For example, do the diodes and transistors refer to only those within one each of the first/second differential circuits, or to all the diodes and transistors within all of the plurality of first/second differential circuits? Also related to these problems within claim 5, does the singular "the common connection point...is connected" (lines 4-5) refer to only a single, common point between one each of the first/second differential circuits, or is there a common point with respect to all of the plurality of first/second differential circuits? Claim 7 has the same type of one/four transistors, four/one diodes, first circuit output terminal, first circuit input terminal, and common connection point problems as claim 5, and therefore they will not be repeated here. It is not clear in claim 8 how the singular first/second differential circuits, and the second circuit input/output terminals relate to the plurality of first/second differential circuits, and to the circuit input/output terminals recited within claim 1. Claim 9 has the same type of problems as claims 5, 7 and/or 8 with respect to one/four transistors, common connection point, four/one diodes, first/second input terminals, first/second output terminals, and the singular first/second differential circuits. Therefore, those problems will also not be described here.

To help clarify the claimed limitations (e.g. series connected differential circuits, what is considered the common connection point, and what are considered the input/output terminals), the examiner requests specific examples of each of those limitations with respect to the plurality of differential circuits shown within the applicant's own figures.

Claim Rejections under 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art arc such that the subject matter as a whole would have been obvious at the time the invention was made to a person having Ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claims 1-3, 5, and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mihailovits et al. (Mihailovits) in view of the teachings of Okanobu. [Both of these references were cited in the previous Office Action.] Fig. 2 of Mihailovits shows a filter circuit comprising three stages 260-280, wherein each stage comprises a pair of differential circuits. The stages are coupled in series between input/output terminals. For example, differential circuits 201,202 and 203,204 of stage 260 receive input signal Vin at input terminals 150,160, and differential circuits 209,210 and 211,212 of stage 280 provide output signal Vout. Therefore, those circuits are deemed to be coupled in series with respect to the input/output terminals. Also, these series coupled stages/differential circuits are also coupled between first and second power supplies (unlabelled but understood to represent a positive power supply and ground). Although Fig. 2 does not show the first and second differential circuits as recited within independent claim 1, each differential circuit (e.g. 201,202) of Fig. 2 can be replaced by the doublet circuit shown in Mihailovits' Fig.5 (see column 3, lines 49-51). The circuit in Fig. 5 shows a first differential circuit comprising one transistor 501 and diode-connected transistor 503 (with an emitter area n-times the area of 501) with their emitter electrodes connected together, wherein a first current (provided by the upper current source IBIAS shown coupled in common to 503 and 504), corresponding to input signal Vin, will flow through diode-connected transistor 503. Also shown in Fig. 5 is a second differential circuit comprising one diode-connected transistor 504 and transistor 502 (with an emitter area n-times the area of 504) with their emitter electrodes connected together, wherein a second current (provided by the upper current source

IBIAS shown coupled in common to 503 and 504), corresponding to input signal Vin, will flow through diode-connected transistor 504. The upper current source IBIAS is coupled to a common connection point of diode-connected transistors 503 and 504. However, the reference of Mihailovits does not show or disclose diode-connected transistor 503 and transistor 502 of Fig. 5 as four parallel connected diode-connected transistors and transistors, respectively. Okanobu shows/discloses three examples of functionally equivalent differential circuits in Figs. 2, 5, and 6. Of special interest, with respect to the present application, differential circuit Q1,Q2 of Fig. 2 (having a ratio of 1:N) corresponds to differential circuit Q1,Q21-Q24 of Fig. 5, wherein the single transistor Q2 (with an emitter area of N) of Fig.2 has been replaced by four (a plurality of) parallel connected transistors Q21-Q24. From the knowledge of one of ordinary skill in the art, and from what Okanobu discloses (e.g. see column 5, line 58 - column 6, line 19), it would have been obvious to one of ordinary skill in the art to replace Mihailovits' diode-connected transistor 503 with an n-number of parallel diode-connected transistors (each having an area A), and also replace transistor 502 with an n-number of parallel. connected transistors (each having an area A). Since Mihailovits discloses the emitter area ratio is typically between 4 and 5 (see column 3 , lines 46-48), it would be understood the ratio typically ranges between 4:1 and 5:1. Therefore, it also would have been obvious to one of ordinary skill in the art to let N = 4, and replace diode-connected transistor 503 with four parallel diode-connected transistors, and also replace transistor 502 with four parallel connected transistors. With such a modification, Mihailovits' Fig. 5 corresponds to the applicant's own Fig. 1 first/second differential circuits 15A/16A. More specifically, Mihailovits' transistors 501,502; diode-connected transistors 503,504, upper current source IBIAS, input Vin, and current sources 505/506 correspond to the applicant's Fig. 1

transistors Q11,Ql 6-Q1 9, diode-connected transistors Q12-Q15,Q20, current source 23A, input VIN+, and current sources 21A/22A, respectively. Referring back to Mihailovits' Fig. 2, with each differential pair shown in Fig. 2 replaced by the modified Fig. 5 circuit, Fig. 5's output Vout (with respect to the replaced differential pair 201,202) would be coupled to the left side of first capacitor 240, and with respect to the replaced differential pair 203,204, it would be coupled to the right side of first capacitor 240. This configuration corresponds to the applicant's Fig. 1 wherein first/second differential circuits 15A/16A, capacitor 17, and first/second differential circuits 15B/16B correspond to Mihailovits' circuit 201,202, capacitor 240, and circuit 203,204, respectively, wherein each of Mihailovits' circuits is replaced by the modified Fig. 5 circuit as previously described. It would also be understood that the current through first capacitor 240 (e.g. shown in Fig. 2 of Mihailovits) would be determined by the upper current source, and the first and second currents flowing through the diode-connected transistors (e.g. 503,504 shown in Fig. 5 of Mihailovits). Using some of the reference designators shown in Fig. 2 to provide a simple example, one of ordinary skill in the art would know circuit 201,202 receives the initial input signal Vin on input terminal 160 and provides an output to circuit 205,206, which in turn provides an output to circuit 209,210 that provides a final output signal Vout. Therefore, it would be obvious to one of ordinary skill in the art that the plurality of corresponding first/second differential circuits are connected in series between the input/output terminals Vin/Vout of Fig. 2, thus rendering claim 1 obvious. Since these series connected circuits are also connected between the first/second power supplies (not labeled but understood to represent a positive power supply voltage and ground), claim 2 is rendered obvious. As shown in Fig. 5, the first differential circuit 501,503 is connected in parallel to the second differential circuit 502,504, thus

rendering claim 3 obvious. It is noted that the corresponding parallel connections would also hold true for the filter circuit shown within Fig. 2. Also shown in Fig. 5, the control electrodes of transistors 501 and 502 (representing four parallel connected transistors as previously described) are connected to a first circuit input terminal Vin, and a common connection of diodes 503 (representing four parallel diode-connected transistors as previously described) and 504 are connected to a first circuit output terminal Vout, wherein one terminal of first capacitor 240 (shown in Fig. 2) is connected to first circuit output terminal Vout (with respect to the replaced circuits 201,202 and 203,204 of Fig. 2. Therefore, claim 5 is rendered obvious. Although not shown or disclosed by Mihailovits, it would have been obvious to one of ordinary skill in the art to replace one of the Vin input terminals of Fig. 2 with a direct-current power supply (e.g. reference voltage). For example, connecting Fig. 2 input terminal 150 to a direct-current power supply instead of Vin, that power supply would be connected to the control electrodes of transistors 501,502 (of Fig. 5) that replaced circuit 203,204. Since the common connection point, and its connection to the first capacitor have previously been described, claim 7 is rendered obvious. The use of a direct-current power supply (e.g. reference voltage) is known as one type of input to a differential circuit. It provides a specific, set reference level at which a differential circuit will trigger when another varying input reaches and/or crosses that level. In this case, circuit 201,202 will receive the variable input signal Vin at input terminal 160, and that will be compared with the direct-current power supply at input terminal 150 via associated circuit 203,204. Second capacitor 241 of Fig. 2 can be deemed connected between a second circuit input terminal and a second circuit output terminal (e.g. a second circuit 205-208 receives a second input signal (from 201-204) and provides a second output signal (to 209-212) at respective

terminals, with capacitor 241 connected between those input/output terminals), thus rendering claims 8 and 9 obvious. The replacement of one transistor (or diode-connected transistor), having a large emitter area, with a plurality of parallel transistors (or diode-connected transistors) is one means of using a functionally equivalent element for another as is known to those of ordinary skill in the art. Therefore, this examiner does not consider the replacement of one circuit/element with a functionally equivalent circuit/element as novel.

No claim is allowable.

Claims 4 and 6 have been cancelled.

Response to Arguments

The applicant's arguments filed Dec 2, 2002 have been fully considered, but they are not persuasive. The applicant argues that: 1) the differential circuits are connected in series with each other; 2) the claimed filter circuit has low-voltage operation, extended input dynamic range, and reduced current consumption; 3) Mihailovits does not mention the four parallel diodes (or diode-connected transistors) or the four parallel transistors; 4) the general knowledge of one of ordinary skill in the art and/or the prior art must provide a suggestion, motivation, teaching, or incentive to make the claimed combination or invention; and 5) there was no motivation to modify Mihailovits' filter circuit at the time the invention was made.

1) The applicant argues that the (claimed) differential circuits are connected in series on page 9 of the amendment. However, the examiner believes the comments themselves, as well as the claimed limitations, are confusing, or at least misleading. For example, the comments cite "It appears that Claim 2 is supported by the specification" and "Claim 2 may be supported by Figures 6 and 7." From the examiner's viewpoint, neither of these statements provides definite

support for the applicant's allegations of the series connection(s). In fact, the comments appear to imply that the claimed limitations are not clearly supported by the specification and figures. For example, the related comments indicate first differential circuits 15A and 16A of the applicant's Fig. 1 are connected in series with each other, and are connected in series between first/second power supplies 13/14. First, circuit 16A is believed to be a second differential circuit instead of the first as the comment implies. Secondly, even though they are shown coupled between the first/second power supplies, they are shown in what is considered a parallel connection instead of a series connection. It is also noted that these Fig. 1 circuits are coupled in parallel with respect to each other, an input terminal, and an output terminal (e.g. they both share a first common connection, to input terminal 11, for receiving input signal VIN+, and they also share a second common connection A to output terminal 18). The comment that Figs. 6 and 7 illustrate modifications of Fig. 1 does not clarify the claimed limitations. The examiner agrees those figures do show circuits with at least some series coupled elements, but they do not show the connections of the differential circuits as understood within the claims. For example, if the first plurality of first differential circuits is considered circuit 15A1 in the applicant's Fig. 6, its elements are connected in series between first/second power supplies VCC/GND, and the same first current (from 23A) will flow through each set of four diode-connected transistors. However, if each set of transistor and four diode-connected transistors is considered a first differential circuit (e.g. Q11-1 and Q12-1-Q15-1), each first differential circuit does not have the one electrode connected to the first electrode of the first transistor as lines 4-5 of claim 1 implies. If the series connection of the first series connection circuit is considered between the input/output terminals (i.e. 11/18), it appears the claimed limitation is misleading with respect to what is

shown in Fig. 6. For example, a series connection between input/output terminals is typically considered a series of elements (or circuits) wherein the output of a preceding element is coupled to the input of a following element with two exceptions: 1) the first element of the series will have its input coupled to the initial input terminal; and 2) the last element of the series will have its output coupled to the final output terminal. Therefore, Fig. 6 falls to show each first differential circuit (of the first series connection circuit) as claim l recites, the series connection between input/output terminals as claim 1 apparently recites, and the series connection of the plurality of differential circuits between the first/second power supplies as recited within claim 2. However, if the applicant's Fig. 7 is considered, a plurality of first differential circuits 15A2-1,15A2-n is shown coupled in series between input/output terminals 11/18. But in this case, only the first current of the last differential circuit 15A2-n flows to first capacitor 17. Therefore, Fig. 7 also fails to support the series connection that is recited, if the current within the first capacitor of claim 1 is meant to receive the first current from each one of the first differential circuits.

2) In response to the applicant's argument that the references fail to show certain features of the applicant's invention, it is noted that the features upon which the applicant relies (i.e. a filter circuit with low-voltage operation, extended input dynamic range, and reduced current consumption) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

3) The examiner agrees that the reference of Mihailovits does not mention the four parallel diodes (or diode-connected transistors) and the four parallel transistors. However, Fig. 5 of Mihailovits clearly shows a structure comprising: a first differential circuit comprising

transistor 501 (with an emitter area of A) and diode-connected transistor 503 (with an emitter area of nA); and a second differential circuit comprising diode-connected transistor 504 (with an emitter area of A) and transistor 502 (with an emitter area of nA). One of ordinary skill in the art would recognize that one transistor having an emitter area of nA, wherein A represents the emitter area of a single transistor, can be replaced with a functionally equivalent n-number of parallel coupled transistors, each having an emitter area A. [This knowledge is supported by the Okanobu reference, cited in the previous Office Action and now incorporated within the formal rejections with respect to Mihailovits. For example, consider Okanobu's transistors Q1/Q2 of Fig. 2; Q1/Q21-Q24 of Fig. 5; and Q1/Q2' of Fig. 6, as well as their descriptions.] Mihailovits also discloses the emitter area ratio is typically between 4 and 5. This is understood to mean the ratio can be from 4:1 to 5:1. Assuming a typical ratio of 4:1, one of ordinary skill in the art would understand that diode-connected transistor 503 would have an area of four times the area of associated transistor 501. Therefore, since diode-connected transistor 503 could be replaced with a functionally equivalent combination of four parallel diode-connected transistors, each having an emitter area of A, claim 1's four diodes connected in parallel would be obvious. It is also noted that the applicants' Fig. 1 actually shows an example of four parallel diode-connected transistors (e.g. Q12-Q15), but in the applicant's Figs. 6 and 7, the four parallel diode-connected transistors are merely shown as a single diode-connected transistor with slightly larger lines representing the collector and emitter (e.g. see Q12-1 to Q15-1 of Fig. 6 and the right transistor within 15A2-1 shown in Fig. 7). Therefore, these symbols indicate that parallel diode-connected transistors can be represented in different ways.

4) The examiner is fully aware that the general knowledge of one of ordinary skill in the art and/or the prior art must provide a suggestion, motivation, teaching, or incentive to make the claimed combination or invention. In this case, there are numerous motivational reasons for rejecting the claims as described: 1) the claimed limitations, with respect to the plurality (or number) of differential circuits and their series connection(s) between input/output terminals, and/or the first/second power supplies, are not clear (e.g. see both the rejections under 35 U.S.C. 112, second paragraph, and the comments under #1, described above); 2) MPEP 2111 states "CLAIMS MUST BE GIVEN THEIR BROADEST REASONABLE INTERPRETATION"; 3) Fig. 2 of Mihailovits clearly shows a filter circuit with a plurality of stages connected in series between input/output terminals (e.g. see input stage 260 and output stage 280), wherein these series connected stages are also connected between first and second power supplies; 4) Mihailovits' Fig. 5 shows first/second differential circuits (i.e. 501,503/502,504) that closely correspond to the applicant's first/second differential circuits (e.g. 15A/16A of Fig. 1), wherein transistors 502 and 503 of Mihailovits have an n-times emitter area; 5) column 3, lines 49-51 refers to Fig. 5 of Mihailovits, and clearly discloses "Substituting this circuit for each differential pair of the circuit shown in Fig. 2", thus providing a teaching to have a plurality of first/second differential circuits within the filter circuit (e.g. Fig. 2 shows six differential pairs, and when each is replaced by the circuit shown in Fig. 5, there will be six each of the first and second differential circuits); and 6) the knowledge of one of ordinary skill in the art with respect to how parallel connected transistors (or diode-connected transistors) relate to a transistor (or diode-connected transistor) with a larger emitter area (e.g. see the reference of Okanobu).

5) Related to #4 above is the applicant's argument that there was no motivation to modify Mihailovits' filter circuit at the time the-invention was made. Mihailovits' patent was issued on Dec 8, 1998, wherein the applicant's own foreign priority date goes back to only Jan 10, 2001. The reference of Okanobu, now used within the claim rejections to support the examiner's obvious type rejection with respect to using parallel connected transistors (or diode-connected transistors) in place of a transistor (or diode-connected transistor) having a larger emitter area, was issued on Oct 23, 1990. Therefore, the prior art references, and the knowledge of one of ordinary skill in the art, were clearly available prior to the time of the invention.

For the reasons described above, the rejections cited within this Office Action, and the previous Office Action, are deemed proper with respect to the claimed invention.

The prior art reference cited on the IDS submitted on Sep 26, 2002 was not seen by the examiner until after the previous Office Action had been mailed. This reference corresponds to the laid-open Japanese patent cited on the disclosure's page 1. It shows/discloses circuits that correspond to the applicant's own Prior Art Figs. 13-15. However, it does not show the four parallel diodes within the first differential circuit, and the four parallel transistors within the second differential circuit, as recited within independent claim 1.

The applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). The applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (703) 308-4817. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiners supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax number for TC 2800 is (703) 872-9318 for communications before a final action has been mailed, and (703) 872-9319 for communications after a final action.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

TLE

Terry L. Englund

24 February 2003

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800